REMARKS

Claims 1-32 were pending in the application. Claims 2, 4, 7, 13-16, 19, 23, 24, and 29-32 have been cancelled. Claims 1, 3, 6, 8-12, 17, 18, 22, 25 and 28 have been amended. Claims 1, 3, 5, 6, 8-12, 17, 18, 20-22 and 25-28 remain pending in the application.

Objections to the Drawings:

The drawings were objected to. In a first objection, the Examiner states that the LSSD clocks and STEP clocks shown in Figure 2 are not referred to in the disclosure. Applicant respectfully disagrees, and submits that both the LSSD clocks (also shown as LSSD_CLKA and LSSD_CLKB in Figure 9) and the STEP clocks (shown in Figure 9 as the clock signals of LBST_STEP_CLKC and LBST_STEP_CLKE) are referred to in the paragraph beginning on page 10, line 6, in conjunction with Figure 9.

The drawings were also objected to because the LSSD_CLKA, LSSD_CLKB, LBST_SCAN_CLKA and LBST_SCAN_CLKB were not referred to in the disclosure. Applicant has amended the disclosure to include reference to the LSSD_CLKA and LSSD_CLKB signals, which are the LSSD clocks discussed above. Applicant has amended Figure 9 to remove the LBST_SCAN_CLKA and LBST_SCAN_CLKB references.

Objection to the Specification:

The specification was objected to for various informalities. Applicant has amended the specification to correct these informalities.

Claim Objections:

Claims 1 and 17 were objected to for informalities. Applicant submits that the amended versions of these claims overcome the Examiner's objections.

35 U.S.C. § 112 Rejection:

Claims 7 and 28 were rejected under 35 U.S.C. § 112, first and second paragraphs. Claim 5 was rejected under 35 U.S.C. § 112, second paragraph. Applicant has cancelled claim 7 and therefore believes its rejection to be moot. Applicant submits the amendment to claim 28 overcomes the 35 U.S.C. § 112 first and second paragraph rejections. With respect to claim 5, Applicant submits that the amendment to claim 1 establishes antecedent basis and therefore obviates the rejection.

35 U.S.C. § 102 and 35 U.S.C. § 103 Rejections:

Claims 1, 13, 16, 22, 26, 28, 29 and 32 were rejected under 35 U.S.C. § 102(e) as being anticipated by Au, U.S. Patent 6,681,359. Claims 2, 6, 7m 8, 17, 19, and 21 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Motika, U.S. Patent 5,982,189, in view of Au. Claims 3, 5, and 18 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Motika in view of Au and in further view of Koproski, U.S. Patent 6,671,838. Claims 4 and 24 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Motika in view of Au and in further view of Koproski, Zuraski, U.S. Patent 6,560,740, Lo, U.S. Patent 5,661,732, and Wong, U.S. Patent 6,636,997. Claims 9 and 11 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Motika in view of Au and in further view of Zuraski. Claims 10, 12, and 27 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Motika in view of Au and in further view of Zuraski and Lo. Claim 14 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Au in view of Motika. Claims 15, 23, 25, 30, and 31 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Au in view of Koproski. Claim 20 was rejected under 35 U.S.C.§ 103(a) as being unpatentable over Motika in view of Au and in further view of Kim, U.S. Patent 6,148,426. With respect to the cancelled claims, Applicant believes the rejections to be moot. With respect to the pending claims, Applicant respectfully traverses this rejection.

With regard to the § 102 rejection, the cited reference does not anticipate the independent claims. With regard to the § 103 rejection, the cited references, taken singly or in combination, do not teach all of the elements of the independent claims.

Motika teaches a built-in stress circuit for an integrated circuit that has a frequency generator, at least one self-test circuit, a temperature regulator and a controller. The frequency generator receives a reference clock and an adjusted temperature frequency from the temperature regulator and outputs the test frequencies needed for the self-test circuits. The self-test circuits, which are coupled to the frequency generator, receive the test frequencies and dissipate power as the self-test circuits are being used. The temperature regulator, which is coupled to the self-test circuits and the frequency generator, senses the power dissipated (i.e., the temperature), adjusts a temperature frequency corresponding to the temperature desired, and outputs the adjusted temperature frequency. The controller, which is coupled to the frequency generator, the self-test circuits, and the temperature regulator, provides the control data necessary for testing both electrical and thermal stress conditions.

Au teaches a circuit, method and a test architecture that may be used for testing one or more integrated circuits that may be arranged upon a printed circuit board. Along with internal logic used by the integrated circuit during normal functioning, circuitry is included for built-in self-test. In an embodiment, the integrated circuits are semiconductor memories and include Memory Built-In Self-Test (MBIST) capability. A JTAG-compliant interface may be used to control the MBIST circuitry so that MBIST test modes can be selected by the JTAG Test Access Port controller, and MBIST test results can be written into boundary scan cells and scanned out through the JTAG Test Data Out port. The addition of a high-speed clock signal to the standard 4-wire JTAG interface allows full-speed operation of the MBIST circuitry. Therefore, the integrated circuit can be tested at full speed, and the test results scanned out by the slower JTAG clock. The use of the JTAG interface with MBIST allows multiple interconnected devices to be tested using a single interface. This is advantageous for in-circuit testing, since it is not necessary to directly probe each device to be tested. It also simplifies the use of automated test equipment, since the JTAG standard is widely used.

Lo teaches a computer system element that has a VLSI array with redundant areas and an ABIST (Array Built-In Self Test system). The ABIST controller allows self test

functions (e.g. test patterns, read/write access, and test sequences) to be used with dual logical views to reduce test time. The ABIST generates pseudo-random address patterns for improved test coverage. A jump-to-third pointer control command enables branching to perform looping after a background has been filled. A data register is divided into multiple sections to enable a Walking/Marching pattern to be executed individually and concurrently in the dual views to further reduce test times.

In contrast, Applicant's independent claim 1 recites, in pertinent part:

"A built-in self-test controller ... wherein the built-in self-test controller is configured to:
enter a reset state;
enter an initiate state entered from the reset state upon receipt of a logic built-in self-test run signal;
scan a scan chain responsive to entering the initiate state;
step to a **new scan chain**; and
repeat the previous scanning and stepping until the content of a pattern generator in the logic built-in self-test engine of the built-in self-test controller equals a predetermined vector count." (Emphasis added).

Independent claims 17 and 22 recite similar combinations of featuers.

Taken singly, Au does not teach or suggest this combination of features, and therefore does not anticipate the independent claims. Furthermore, Applicant submits that taken singly or in combination, the cited references do not teach or suggest all of the elements of the independent claims, and that the claims are therefore not rendered obvious. In the office action, the Examiner states, that Lo teaches, in column 6, lines 26-50, the states of scan, step, and complete as specified in the claims. However, Applicant submits that Lo does not teach or suggest a built-in self-test controller configured to step to a **new scan chain**, as recited in claim 1, or similarly recited in the other independent

claims. Applicant can find no teaching or suggestion of this combination of features anywhere in Lo or in any of the other cited references.

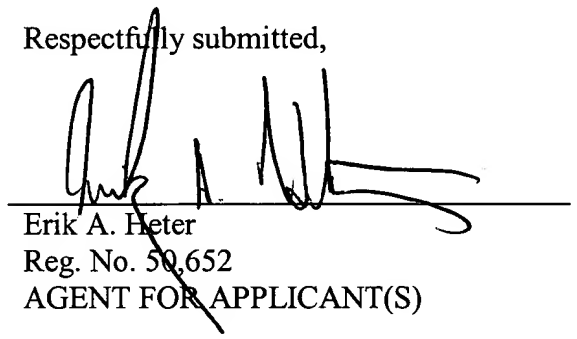
In light of the above remarks, Applicant submits that neither the standard for anticipation nor the standard for obviousness has been met. Accordingly, removal of the 35 U.S.C. § 102(e) and the 35 U.S.C. § 103(a) rejections is respectfully requested.

CONCLUSION

Applicant submits the application is in condition for allowance, and an early notice to that effect is requested.

If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5681-55400/BNK.

Respectfully submitted,



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